

FIGURE 1-1: PIC16F630/676 BLOCK DIAGRAM

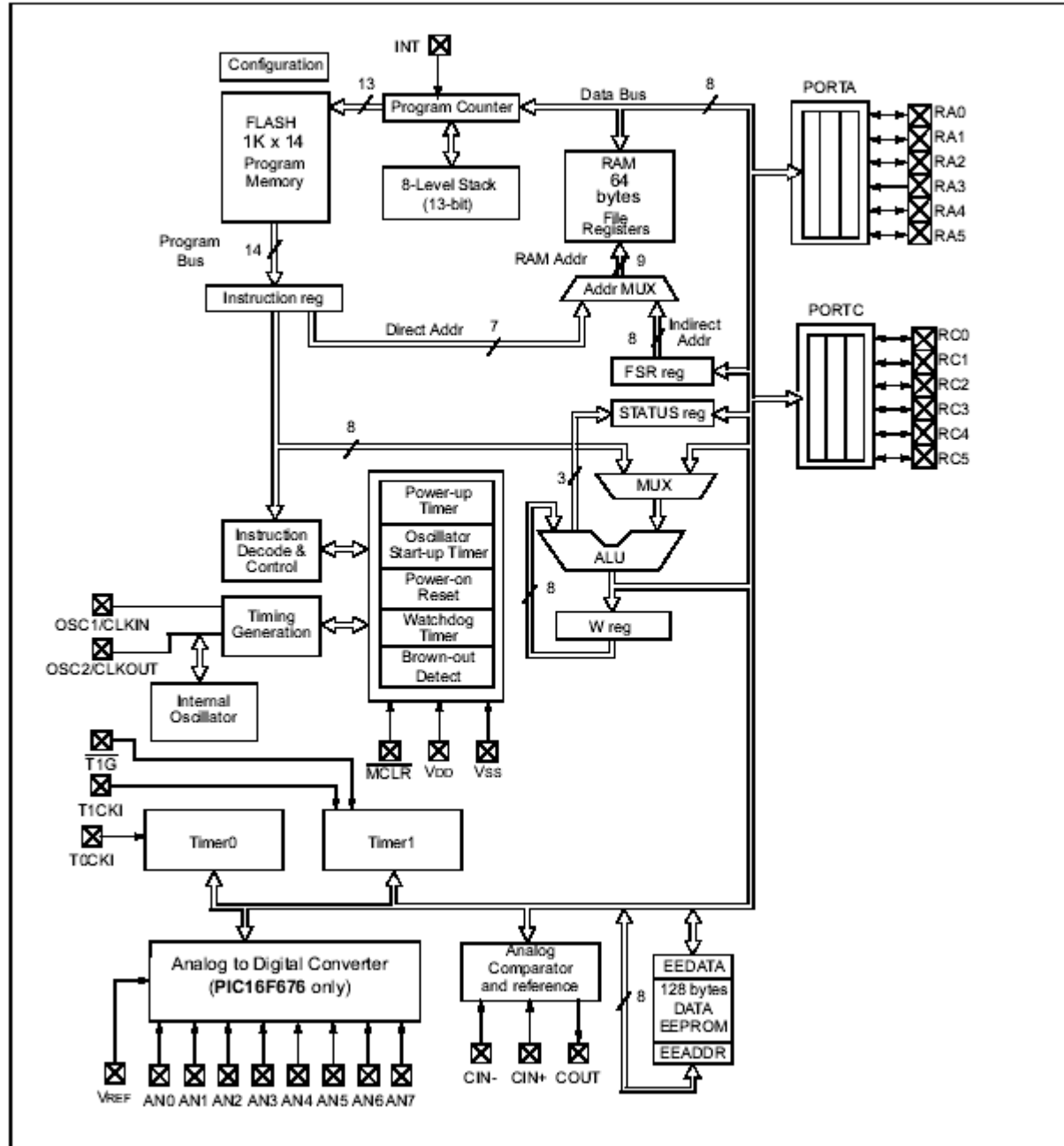
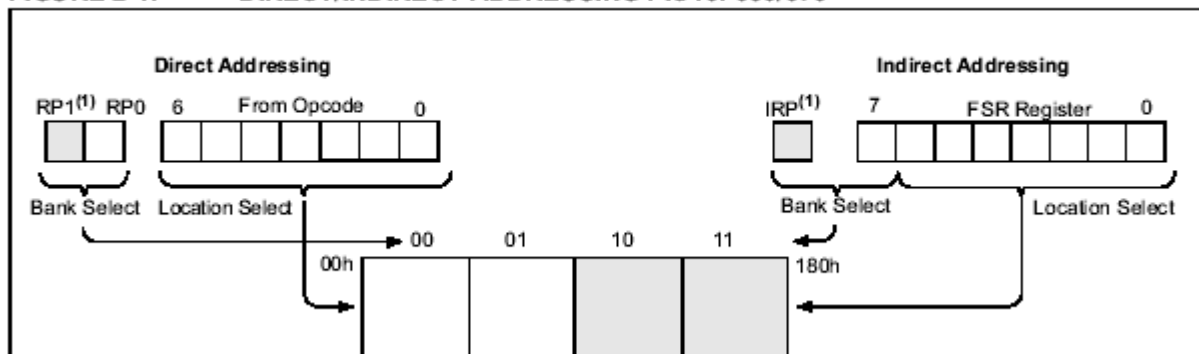


FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F630/676



PIC16F630/676

14-Pin FLASH-Based 8-Bit CMOS Microcontroller

High Performance RISC CPU:

- Only 35 instructions to learn
- All single cycle instructions except branches
- Operating speed:
 - DC - 20 MHz oscillator/clock input
 - DC - 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:

- Internal and external oscillator options
 - Precision Internal 4 MHz oscillator factory calibrated to $\pm 1\%$
 - External Oscillator support for crystals and resonators
- 5 μs wake-up from SLEEP, 3.0V, typical
- Power saving SLEEP mode
- Wide operating voltage range - 2.0V to 5.5V
- Industrial and Extended temperature range
- Low power Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD)
- Watchdog Timer (WDT) with independent oscillator for reliable operation
- Multiplexed MCLR/Input-pin
- Interrupt-on-pin change
- Individual programmable weak pull-ups
- Programmable code protection
- High Endurance FLASH/EEPROM Cell
 - 100,000 write FLASH endurance
 - 1,000,000 write EEPROM endurance
 - FLASH/Data EEPROM Retention: > 40 years

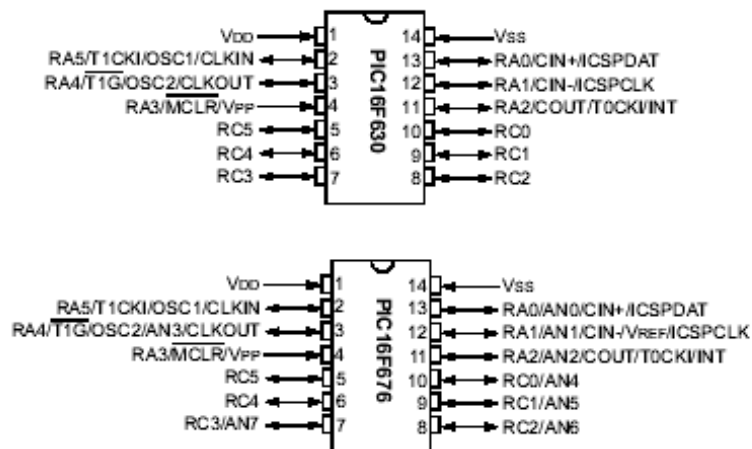
Low Power Features:

- Standby Current:
 - 1 nA @ 2.0V, typical
- Operating Current:
 - 8.5 μA @ 32 kHz, 2.0V, typical
 - 100 μA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current
 - 300 nA @ 2.0V, typical
- Timer1 oscillator current:
 - 4 μA @ 32 kHz, 2.0V, typical

Peripheral Features:

- 12 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
 - One analog comparator
 - Programmable on-chip comparator voltage reference (CVREF) module
 - Programmable input multiplexing from device inputs
 - Comparator output is externally accessible
- Analog-to-Digital Converter module (PIC16F676):
 - 10-bit resolution
 - Programmable 8-channel input
 - Voltage reference input
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
 - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- In-Circuit Serial Programming™ (ICSP™) via two pins

14-pin PDIP, SOIC, TSSOP



INSTRUCTION SET SUMMARY

OPCODE FIELD DESCRIPTIONS

Field Description

- f Register file address (0x00 to 0x7F)
- w Working register (accumulator)
- b Bit address within an 8-bit file register
- k Literal field, constant data or label
- x Don't care location (= 0 or 1).

The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
 d Destination select; d = 0: store result in W, d = 1: store result in file register f.
 Default is d = 1.

GENERAL FORMAT FOR INSTRUCTIONS

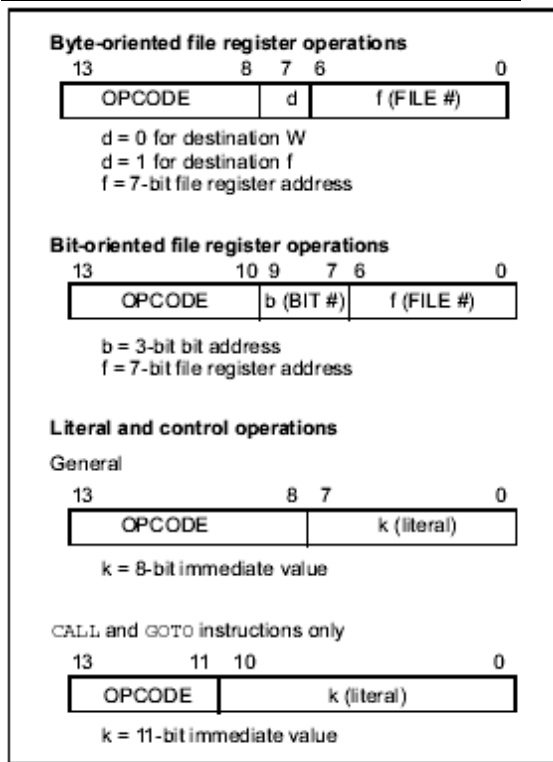


FIGURE 2-2: DATA MEMORY MAP OF THE PIC16F630/676



Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes	
			MSb	LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00	0001 1fff ffff	Z	2
CLRWF	-	Clear W	1	00	0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00	1001 dfff ffff	Z	1,2
DECf	f, d	Decrement f	1	00	0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00	1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000 1fff ffff		
NOP	-	No Operation	1	00	0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	f, b	Bit Clear f	1	01	00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS							
ADDLW	k	Add literal and W	1	11	111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000 0110 0100	<u>TO,PD</u>	
GOTO	k	Go to address	2	10	1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00	0000 0000 1001		
RETLW	k	Return with literal in W	2	11	01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00	0000 0000 1000		
SLEEP	-	Go into Standby mode	1	00	0000 0110 0011	<u>TO,PD</u>	
SUBLW	k	Subtract W from literal	1	11	110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010 kkkk kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVWF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, $d = 1$), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.